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10/661,492	09/15/2003	Chu-Ting Su	REAP0480USA	9226

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EXAMINER	
LAO, LUN S	

ART UNIT	PAPER NUMBER
2614	

NOTIFICATION DATE	DELIVERY MODE
08/07/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/661,492	SU ET AL.	
	Examiner	Art Unit	
	LUN-SEE LAO	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-26,29-35 and 38-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-26,29-35 and 38-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This action is in response to the remarks filed on 04-29-2009. Claims 1-23, 27-28 and 36-37 have been canceled. Claims 24-26, 29-35 and 38- 43 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 24-26, 29-33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson et al (US 2004/0081099).

Consider claim 24, Patterson teaches an apparatus for automatically determining a type of an external device (see fig.1), comprising:

a jack (see fig.1, 2 (26)) for coupling the external device (24); an impedance detecting circuit (30,32), coupled to the external device (24) through the jack (26), for generating a first analog signal according to an impedance of the external device (see fig. 9B (jack)) and a first resistance (R1), a second analog signal according to the impedance of the external device (jack) and a second resistance (R5) and a third analog signal according to the impedance of the external device and a third resistance (R6), wherein the first, second and third resistances (75 ohm, 4.7k ohm and 300 ohm) are different;

an analog-to-digital converter (see fig.4 (36) and page 4 [0049]), coupled to the impedance detecting circuit, for converting the first, second and third analog signals to a first, second and third digital values, respectively; and

a control circuit (see fig.1 (12, 30, 32)), coupled to the analog-to-digital converter (30, 32 and see page4 [0046]-[0049]), for determining the type of the external device (24) when the first digital value falls within a first predetermined range (see fig.5 (146)), the second digital value falls within a second predetermined range (150 in fig.5), the third digital value falls within a third predetermined range (154 in fig.5) and all of the first, second and third predetermined ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions (148,152, 158 and 160 in fig.5 and see page 5 [0055]); wherein the impedance detecting circuit comprises a plurality of resistors, which couples together in parallel, for providing the first, second and third resistance (see fig.9B (R1 (75 ohm), R5 (4.7k ohm) and R6 (300 ohm) and page 7 [0059]) and each of the first, second and third digital values is a number (see figs.9A, 9B, 10 (JS0,JS1, JS3) and page 7 [0059]-[0062]).

While Patterson does not explicitly teach that the number is a multi-bit number, Patterson teaches that the decision tree can be implemented in hardware and/or software ([0031], [0055]). One of ordinary skill in the art would recognize that the decision tree of fig.5 is equivalent to the jack sensing table of fig. 10 (see page 6 [0059]). Considering the flexibility of computer software programming, it would have been obvious to implement, via software programming, the number as a multi-bit number of digital values, for the ease of configuration.

Consider claims 25-26, Patterson teaches the apparatus wherein the impedance detecting circuit comprises:

a switching circuit (See fig.9B) for selectively coupling at least one of the resistors to the external device and thereby sequentially generating the first, second and third analog signals which are respectively converted into the first, second and third analog signals which are respectively converted into the first, second and third values by the analog-to-digital converter (see fig.4 (34,36) and page 4 [0049]); and wherein at least two of the first, second and third predetermined ranges are different (148, 152, 158 and 160 in fig.5 and see page 5 [0055]).

Consider claim 29-31, Patterson teaches a connection detecting circuit, coupled between the jack and the impedance detecting circuit, for determining whether the external device couples to the jack such that the impedance detecting circuit generates the first, second and third analog signals when the connection detecting circuit determines the external device being coupled to the jack (see fig.9B and page 7 [0059]); and the control circuit disconnects the coupling relation between the impedance detecting circuit and the jack after determining the type of the external device (see figs. 9A, 9B, 10 and page 7 [0059]-[0062]); and a multiplexing circuit for coupling the external device to an internal circuit according to the type of the external device determined by the control circuit (see fig. 17; and page 5 [0057] and page 7 [0069]-[0073]).

Consider claim 32, Patterson teaches that a decoder, coupled to the control circuit, for receiving a first number of outputs from the control circuit and thereby

generating a second number of outputs; wherein the second number is larger than the first number (146,150 in fig. 5 and see page 5 [0055]).

Consider claim 33, Patterson teaches a method for automatically determining a type of an external device, comprising:

providing a plurality of predetermined resistances by a. plurality of resistors coupled together in parallel (see fig. 9B (R1, R5 and R6));

generating a first analog signal (R1) according to a first coupling relation between the plurality of predetermined resistance and an impedance of the external device (plug);

generating a second analog signal (R5) according to a second coupling relation, which is different from the first coupling relation, between the plurality of predetermined resistances and the impedance of the external device;

generating a third analog signal (R6) according to a third coupling relation, which is different from the first end second coupling relations, between the plurality of predetermined resistances and the impedance of the external device (see fig. 9B (R1, R5 and R6) and page 7 [0059]); respectively converting the first, second and third analog signals to first, second and third digital values (see fig.4 (34, 36) and page 4 [0049]); and

determining the type of the external device when the first digital value falls within a first predetermined range (see fig.5 (146)), the second digital value falls within a second predetermined range (150 in fig.5), the third digital value falls within a third predetermined range (154 in fig.5) and all of the first, second and third ranges together indicate a same recognized condition among a plurality of predetermined recognized

conditions (148, 152, 158 and 160 in fig.5 and see page 5 [0055]); wherein each of the first, second and third digital values is a number (see figs.9A, 9B, 10 (JS0,JS1, JS3) and page 7 [0059]-[0062]).

While Patterson does not explicitly teach that the number is a multi-bit number, Patterson teaches that the decision tree can be implemented in hardware and/or software ([0031], [0055]). One of ordinary skill in the art would recognize that the decision tree of fig.5 is equivalent to the jack sensing table of fig. 10 (see page 6 [0059]). Considering the flexibility of computer software programming, it would have been obvious to implement, via software programming, the number as a multi-bit number of digital values, for the ease of configuration.

Consider claim 35, Patterson teaches wherein at least two of the first, second and third predetermined rang are different (146,150, 154 in fig.5 and see page 5 [0055]).

4. Claims 34 and 38-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson et al (US 2004/0081099) in view of Dao (US PAT. 6,407,633).

Consider claim 34, Patterson teaches the method further comprising:

decoupling a first resistor of the plurality of resistors from the impedance of the external device before coupling second resistor of plurality of resistors to the impedance of the external device (see fig. 9B and page 7 [0059]); but Patterson does not explicitly teach decoupling the second resistor from the impedance of the external device before

coupling a third resistor of the plurality of resistors to the impedance of the external device; and

decoupling all of the plurality of resistors from the impedance of the external device after constituting the recognized condition.

However, Dao teaches decoupling the second resistor from the impedance of the external device before coupling a third resistor of the plurality of resistors to the impedance of the external device; and

decoupling all of the plurality of resistors from the impedance of the external device after constituting the recognized condition (see fig.3, and col. 3 line 35-67 and col. 7 line 20 - col. 8 line 12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Dao into the teaching of Patterson to provide better sound quality for each channel.

Consider claim 38, Patterson teach an apparatus for determining a type of an external device, comprising:

a jack for coupling the external device (see fig. 9B (jack));

an impedance detecting circuit (see fig. 9B (32)), coupled to the external device through the jack (jack), for generating a first analog signal according to an impedance of the external device and a first resistance (R1), a second analog signal according to the impedance of the external device and a second resistance (R5) and a third analog signal according to the impedance of the external device and a third resistance (R6), the impedance detecting circuit comprising:

a plurality of detecting paths coupled together in parallel (see fig. 9B (R1, R5 and R6) and page 7 [0059]),

an analog-to-digital converter (see fig. 4 (34, 36) and page 4 [0049]), coupled to the impedance detecting circuit, for converting the first, second and third analog signals to a first, second and third digital values; and

a control circuit (see fig.1 (CPU)), coupled to the analog-to-digital converter (30, 32 and see page4 [0046]-[0049]), for determining the type of the external device (24) when the first digital value falls within a first predetermined range (see fig. 5 (146)), the second digital value falls within a second predetermined range (150 in fig. 5), the third digital value falls within a third predetermined range (154 in fig. 5) and all of the first, second and third predetermined ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions (148,152, 158 and 160 in fig.5 and see page 5 [0055]); wherein the first, second and third resistance are different (see fig. 9B (R1 (75 ohm), R5 (4.7k ohm) and R6 (300 ohm) and page 7 [0059]) and each of the first, second and third digital values is a multi-bit number (see figs. 9A, 9B, 10 (JS0,JS1, JS3) and page 7 [0059]-[0062]) (Refer to claim 24 for a discussion of the multi-bit number); but Patterson does not explicitly teach each of the detecting paths comprising a resistor and a transistor coupled together in series, and on/off conditions of the transistors determining the first, second and third resistances.

However, Dao teaches each of the detecting paths comprising a resistor and a transistor coupled together in series, and on/off conditions of the transistors determining

the first, second and third resistances (see fig.3, and col. 3 line 35-67 and col. 7 line 20-col. 8 line 12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Dao into the teaching of Patterson to provide better sound quality for each channel.

Consider claim 39, Patterson as modified by Dao teaches the apparatus wherein the plurality of detecting paths comprises:

a first detecting path comprising a first resistor and a first transistor coupled in series; a second detecting path, coupled to the first detecting path in parallel, comprising a second resistor and a second transistor coupled in series; and a third detecting path, coupled to the first and second paths in parallel, comprising a third resistor and a third transistor coupled in series; wherein the first resistance is determined when the first transistor is switched on and the second and third transistors are switched off, the second resistance is determined when the second transistor is switched on and the first and third transistors are switched off and the third resistance is determined when the third transistor is switched on and the first and second transistors are switched off (Dao, see fig.3, and col. 3 line 35-67 and col. 7 line20 - col. 8 line 12 and Patterson, see figs. 10, 15-17; and page 6 [0060] and page 7 [0069]-[0073]).

Consider claim 40, Patterson as modified by Dao teaches the apparatus further comprising:

a connection detecting circuit (see fig. 17 (410b)), coupled between the jack (jack) and the impedance detecting circuit (410), for determining whether the external

device couples to the jack such that the impedance detecting circuit generates the first, second and third analog signals when the connection detecting circuit determines the external device being coupled to the jack (see fig. 17; and page 6 [0060] and page 7 [0069]-[0073]).

Consider claims 41-43, Patterson as modified by Dao teaches the apparatus wherein the control circuit disconnects the coupling relation between the impedance detecting circuit and the jack after determining the type of the external device (see fig. 17; and page 6 [0060] and page 7 [0069]-[0073]); and the apparatus further comprising: a multiplexing circuit for coupling the external device to an internal circuit, according to the type of the external device determined by file control circuit (see figs. 4, 7, 17; and page 5 [0057] and page 7 [0069]-[0073]); and the apparatus further comprising: a decoder (see fig. 17 (412)), coupled to the control circuit (11), for receiving a first number of outputs from the control circuit and thereby generating a second number of outputs; wherein the second number is larger than the first number (see fig. 5; and page 6 [0060] and page 7 [0069]-[0073]).

Response to Arguments

5. Applicant's argumenst regarding the rejection under 35 U.S.C. 112, first paragraph been fully considered and found to be persuasive.

6. Regarding the prior art rejections, applicant's arguments with respect to claims 24-26, 29-35 and 38- 43 have been fully considered but they are not persuasive.

Applicant argued that Patterson fails to teach an impedance detecting circuit, coupled to the external device through the jack, for generating a first analog signal according to an impedance of the external device and a first resistance, a second analog signal according to the impedance of the external device and a second resistance and a third analog signal according to the impedance of the external device and a third resistance, wherein the first, second and third resistances are different (Remarks, page 12, third paragraph – page 13, first paragraph).

The examiner respectfully disagrees. Patterson discloses a jack (see fig. 1, 2 (26)) for coupling the external device (24); an impedance detecting circuit (30, 32), coupled to the external device (24) through the jack (26), for generating a first analog signal according to an impedance of the external device (see fig. 9B (jack)) and a first resistance (R1), a second analog signal according to the impedance of the external device (jack) and a second resistance (R5) and a third analog signal according to the impedance of the external device and a third resistance (R6), wherein the first, second and third resistances are different (see fig. 9B (R1 (75 ohm), R5 (4.7k ohm) and R6 (300 ohm)) and page 7 [0059]). One of ordinary skill in the art would recognize that an external device (speaker, headphone, microphone, or nothing, listed in fig. 10) inherently has an impedance value. The signal which is input to 260 (fig. 9B) is affected by / dependent on both the impedance corresponding to R1 and the impedance corresponding to that of the external device because both are in the signal path which results in the signal which is input to 260. In other words, the impedance detecting circuit of Patterson generates a first signal (signal which is input to 260) according to an

impedance of the external device (the inherent impedance of the external device) and a first resistance (R1). The same is true for the second signal and the third signal. On the other hand, a detecting signal is generated according to R1, the signal is generated according to the impedance of the external device. It meets the limitations as recited in 24.

Applicant further argued that Patterson fails to teach generating three analog signals in the reconfiguration circuit according to the impedance of the external device concurrently with three different resistances (Remarks, page 13, first paragraph).

The examiner responds that the argued concurrency is not claimed, and thus moot. For the reasons explained above, Patterson teaches generating three analog signals in the reconfiguration circuit according to the impedance of the external device and the three different resistances/impedances.

Applicant further argued that Patterson fails to teach analog to digital converter for converting the first, second and third analog signals to a first, second and third digital values, respectively (Remarks, page 13, 2nd paragraph).

The examiner respectfully disagrees. In Patterson, the reconfiguration circuit block 32e of fig. 9B corresponds to the reconfiguration circuit block 32b of fig. 4, which clearly shows that the signal generated in the reconfiguration circuit block 32e/b is input into the analog-digital converter 124. Each of the first/second/third signals is converted in this manner in Patterson.

Applicant further argued that Patterson fails to teach "a control circuit for determining the type of an external device when a first digital value converted from the

first analog signal falls within a first predetermined range, a second digital value converted from the second analog signal falls within a second predetermined range, the third digital value converted from the third analog signal falls within a third predetermined range and all of the first second and third predetermined ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions; wherein each of the first, second and third digital values is a multi-bit number" (Remarks, pages 14-15).

The examiner respectfully disagrees. Patterson discloses a control circuit (see fig.1 (12, 30, 32)), coupled to the analog-to-digital converter (30, 32 and see page 4 [0046]-[0049]), for determining the type of the external device (24) when the first digital value falls within a first predetermined range (see fig. 5 (146)), the second digital value falls within a second predetermined range (150 in fig.5), the third digital value falls within a third predetermined range (154 in fig.5) and all of the first, second and third predetermined ranges together indicate a same recognized condition among a plurality of predetermined recognized conditions (148,152, 158 and 160 in fig. 5 and see page 5 [0055]); wherein the impedance detecting circuit comprises a plurality of resistors, which couples together in parallel, for providing the first, second and third resistance (see fig. 9B (R1, R5 and R6 and page 7 [0059]) and each of the first, second and third digital values is a number (see figs.9A, 9B, 10 (JS0,JS1, JS3) and page 7 [0059]-[0062]). While Patterson does not explicitly teach that the number is a multi-bit number, Patterson teaches that the decision tree can be implemented in hardware and/or software ([0031], [0055]). One of ordinary skill in the art would recognize that the

decision tree of fig.5 is equivalent to the jack sensing table of fig. 10 (see page 6 [0059]). Considering the flexibility of computer software programming, it would be obvious to implement, via software programming, the number as a multi-bit number of digital values, for the ease of configuration. It is this modified teaching of Patterson that meets the control circuit for determining as claimed.

For at least these reasons, applicant's arguments regarding Patterson are not persuasive.

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kim et al. (US PAT. 6,397,087) is cited to show other related apparatus for automatic identification of audio input/output device and method thereof.

9. Any response to this action should be mailed to:

Mail Stop ____(explanation, e.g., Amendment or After-final, etc.)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Facsimile responses should be faxed to:
(571) 273-8300

Hand-delivered responses should be brought to:
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Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lao,Lun-See whose telephone number is (571) 272-7501 The examiner can normally be reached on Monday-Friday from 8:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin, can be reached on (571) 272-7848.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 whose telephone number is (571) 272-2600.

Lao, Lun-See
/Lun-See Lao/
Examiner, Art Unit 2614
Patent Examiner
US Patent and Trademark Office
Knox
571-272-7501

Date 08-01-2009

/Vivian Chin/
Supervisory Patent Examiner, Art Unit 2614